Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **IN1**
2. **OUT1**
3. **OUT2**
4. **IN2**
5. **C2**
6. **C3**
7. **VSS**
8. **IN3**
9. **OUT3**
10. **OUT4**
11. **IN4**
12. **C4**
13. **C1**
14. **VDD**

**.054”**

**.060”**

**2 1 14 13**

**3**

**4**

**5**

**6 7 8 9**

**12**

**11**

**10**

**MC14Ø66**

**MASK**

**REF**

**BT7**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: MC14Ø66**

**APPROVED BY: DK DIE SIZE .054” X .060” DATE: 12/2/21**

**MFG: MOTOROLA THICKNESS .013” P/N: CD4066B**

**DG 10.1.2**

#### Rev B, 7/1